I CLAIM:

1. Apparatus for processing data, said apparatus comprising:

a plurality of processors operable to execute respective streams of program instructions, said respective streams of program instructions being separate processing threads within a multi-processing environment; and

a clock speed controller operable to select one of a plurality of different non-zero clock speeds as a clock signal controlling execution of program instructions by at least one of said processors, whereby said clock speed may be reduced by said clock speed controller to reduce energy consumption of said apparatus in accordance with a required processing rate of said apparatus.

2. Apparatus as claimed in claim 1, wherein said clock speed controller is operable to dynamically select said clock signal to have a desired clock speed.

3. Apparatus as claimed in claim 2, wherein said clock speed controller is responsive to a detected level of parallelism between respective streams of program instructions to dynamically select said clock signal.

4. Apparatus as claimed in claim 3, comprising a parallelism detector being one of:

a hardware circuit detecting parallel processing activity of said plurality of processors; and

one of said processors executing a parallelism detecting algorithm.

5. Apparatus as claimed in claim 3, wherein said clock speed controller is responsive to a detected level of thread level parallelism.

6. Apparatus as claimed in claim 5, wherein said detected level of thread level parallelism includes parallelism between independent processes and parallelism within a single process.

7. Apparatus as claimed in claim 5, wherein said thread level parallelism is a measure of how many parallel threads are executing for periods when at least one thread is executing.

8. Apparatus as claimed in claim 1, wherein said plurality of processors are operable to execute respective streams of program instructions under control of a respective clock signal having a plurality of different clock speeds.

9. Apparatus as claimed in claim 8, wherein said plurality of processors share a common clock speed and a common clock source.

10. Apparatus as claimed in claim 8, wherein said plurality of processors have independently adjustable clock speeds.

11. Apparatus as claimed in claim 1, wherein said plurality of processors are formed on a single integrated circuit.

12. Apparatus as claimed in claim 1, wherein said clock speed controller comprises at least one of said processors executing a clock speed controlling algorithm.

13. Apparatus as claimed in claim 12, wherein said clock speed controlling algorithm is part of an operating system kernel.

14. Apparatus as claimed in claim 13, wherein said operating system kernel is distributed between said plurality of processors.

15. Apparatus as claimed in claim 1, wherein said apparatus has a maximum required processing workload and when operating below said maximum required processing workload said clock speed controller selects a clock speed less than a maximum clock speed for said at least one processor.

16. Apparatus as claimed in claim 1, wherein said clock speed controller is also operable to control a supply voltage level for said at least one processor such that said supply voltage level is reduced as said clock speed is reduced.

17. Apparatus as claimed in claim 16, wherein said clock speed controller is operable such that processors operating at different clock speeds are provided with different supply voltage levels.

18. Apparatus as claimed in claim 3, wherein said clock speed controller is responsive to a determination of a potential level of parallelism above a threshold level of parallelism to wake a processor from a sleep mode into a clock mode such that said processor may execute a parallel stream of program instructions.

19. Apparatus as claimed in claim 1, wherein said plurality of processors are a plurality of general purpose processor cores.

20. Apparatus as claimed in claim 1, wherein said plurality of processors include at least one of:

a general purpose processor;
a reconfigurable processor;
a hardware accelerator engine;
an application specific processor; and
a digital signal processor.

21. Apparatus as claimed in claim 3, wherein said clock speed controller is operable to reduce a clock speed of at least one processor when said detected level of parallelism has fallen below a threshold level for more than a threshold amount of time.

22. Apparatus as claimed in claim 18, wherein said clock speed controller is operable to speculatively wake said processor from said sleep mode to determine a level of parallelism that may be achieved.

23. A method of processing data, said method comprising the steps of:

executing a plurality of streams of program instructions with respective ones of a plurality of processors, said plurality of streams of program instructions being separate processing threads within a multi-processing environment; and

selecting with a clock speed controller one of a plurality of different non-zero clock speeds as a clock signal controlling execution of program instructions by at least one of said processors, whereby said clock speed may be reduced by said clock speed controller to reduce energy consumption of said plurality of processors in accordance with a required processing rate of said plurality of processors.

24. A method as claimed in claim 23, wherein said clock speed controller is operable to dynamically select said clock signal to have a desired clock speed.

25. A method as claimed in claim 24, wherein said clock speed controller is responsive to a detected level of parallelism between respective streams of program instructions to dynamically select said clock signal.

26. A method as claimed in claim 25, comprising detecting parallelism with a parallelism detector being one of:

a hardware circuit detecting parallel processing activity of said plurality of processors; and

one of said processors executing a parallelism detecting algorithm.

27. A method as claimed in claim 25, wherein said clock speed controller is responsive to a detected level of thread level parallelism.

28. A method as claimed in claim 27, wherein said detected level of thread level parallelism includes parallelism between independent processes and parallelism within a single process.

29. A method as claimed in claim 27, wherein said thread level parallelism is a measure of how many parallel threads are executing for periods when at least one thread is executing.

30. A method as claimed in claim 23, wherein said plurality of processors are operable to execute respective streams of program instructions under control of a respective clock signal having a plurality of different clock speeds.

31. A method as claimed in claim 30, wherein said plurality of processors share a common clock speed and a common clock source.

32. A method as claimed in claim 30, wherein said plurality of processors have independently adjustable clock speeds.

33. A method as claimed in claim 23, wherein said plurality of processors are formed on a single integrated circuit.

34. A method as claimed in claim 23, wherein said clock speed controller comprises at least one of said processors executing a clock speed controlling algorithm.

35. A method as claimed in claim 34, wherein said clock speed controlling algorithm is part of an operating system kernel.

36. A method as claimed in claim 35, wherein said operating system kernel is distributed between said plurality of processors.

37. A method as claimed in claim 23, wherein said plurality of processors have a maximum required processing workload and when operating below said maximum required processing workload said clock speed controller selects a clock speed less than a maximum clock speed for said at least one processor.

38. A method as claimed in claim 23, wherein said clock speed controller is also operable to control a supply voltage level for said at least one processor such that said supply voltage level is reduced as said clock speed is reduced.

39. A method as claimed in claim 38, wherein said clock speed controller is operable such that processors operating at different clock speeds are provided with different supply voltage levels.

40. A method as claimed in claim 25, wherein said clock speed controller is responsive to a determination of a potential level of parallelism above a threshold level of parallelism to wake a processor from a sleep mode into a clock mode such that said processor may execute a parallel stream of program instructions.

41. A method as claimed in claim 23, wherein said plurality of processors are a plurality of general purpose processor cores.

42. A method as claimed in claim 23, wherein said plurality of processors include at least one of:

a general purpose processor;
a reconfigurable processor;
a hardware accelerator engine;
an application specific processor; and
a digital signal processor.

43. A method as claimed in claim 25, wherein said clock speed controller is operable to reduce a clock speed of at least one processor when said detected level of parallelism has fallen below a threshold level for more than a threshold amount of time.

44. A method as claimed in claim 40, wherein said clock speed controller is operable to speculatively wake said processor from said sleep mode to determine a level of parallelism that may be achieved.

45. A computer program product including a computer program operable to control a plurality of processors, said plurality of processors being operable to execute respective streams of program instructions, said respective streams of program instructions being separate processing threads within a multi-processing environment wherein said computer program comprises:

clock speed controlling code operable to select one of a plurality of different non-zero clock speeds as a clock signal controlling execution of program instructions by at least one of said processors, whereby said clock speed may be reduced by said clock speed controlling code to reduce energy consumption of said plurality of processors in accordance with a required processing rate of said plurality of processors.

46. A computer program product as claimed in claim 45, wherein said clock speed controlling code is operable to dynamically select said clock signal to have a desired clock speed.

47. A computer program product as claimed in claim 46, wherein said clock speed controlling code is responsive to a detected level of parallelism between respective streams of program instructions to dynamically select said clock signal.

48. A computer program product as claimed in claim 47, comprising detecting parallelism with a parallelism detector being one of:

a hardware circuit detecting parallel processing activity of said plurality of processors; and

one of said processors executing a parallelism detecting algorithm.

49. A computer program product as claimed in claim 47, wherein said clock speed controlling code is responsive to a detected level of thread level parallelism.

50. A computer program product as claimed in claim 49, wherein said detected level of thread level parallelism includes parallelism between independent processes and parallelism within a single process.

51. A computer program product as claimed in claim 49, wherein said thread level parallelism is a measure of how many parallel threads are executing for periods when at least one thread is executing.

52. A computer program product as claimed in claim 45, wherein said plurality of processors are operable to execute respective streams of program instructions under control of a respective clock signal having a plurality of different clock speeds.

53. A computer program product as claimed in claim 52, wherein said plurality of processors share a common clock speed and a common clock source.

54. A computer program product as claimed in claim 52, wherein said plurality of processors have independently adjustable clock speeds.

55. A computer program product as claimed in claim 45, wherein said plurality of processors are formed on a single integrated circuit.

56. A computer program product as claimed in claim 45, wherein said clock speed controlling code comprises a clock speed controlling algorithm executed by at least one of said processors.

57. A computer program product as claimed in claim 56, wherein said clock speed controlling algorithm is part of an operating system kernel.

58. A computer program product as claimed in claim 57, wherein said operating system kernel is distributed between said plurality of processors.

59. A computer program product as claimed in claim 45, wherein said plurality of processors have a maximum required processing workload and when operating below said maximum required processing workload said clock speed controller selects a clock speed less than a maximum clock speed for said at least one processor.

60. A computer program product as claimed in claim 45, wherein said clock speed controlling code is also operable to control a supply voltage level for said at least one processor such that said supply voltage level is reduced as said clock speed is reduced.

61. A computer program product as claimed in claim 59, wherein said clock speed controlling code is operable such that processors operating at different clock speeds are provided with different supply voltage levels.

62. A computer program product as claimed in claim 47, wherein said clock speed controlling code is responsive to a determination of a potential level of parallelism above a threshold level of parallelism to wake a processor from a sleep mode into a clock mode such that said processor may execute a parallel stream of program instructions.

63. A computer program product as claimed in claim 45, wherein said plurality of processors are a plurality of general purpose processor cores.

64. A computer program product as claimed in claim 45, wherein said plurality of processors include at least one of:

a general purpose processor;
a reconfigurable processor;
an application specific processor; and
a digital signal processor.

65. A computer program product as claimed in claim 47, wherein said clock speed controlling code is operable to reduce a clock speed of at least one processor when said detected level of parallelism has fallen below a threshold level for more than a threshold amount of time.

66. A computer program product as claimed in claim 62, wherein said clock speed controlling code is operable to speculatively wake said processor from said sleep mode to determine a level of parallelism that may be achieved.